Attorney Docket No. 09792909-5828

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Patent Application of: Takeo Eguchi			
Application No:	10/790,986	Group Art Unit:	2193
Filed:	March 2, 2004	Examiner	Chat C. Do
Customer No.:	26263		
For:	SIGNAL PROCESSING AND ERROR ACCUMULATION REDUCING APPARATUS, STORAGE MEDIUM STORING THEREON COMPUTER READABLE CODES TO CONTROL THE SIGNAL PROCESSING AND ERROR ACCUMULATION REDUCING APPARATUS, AND SIGNAL		

Via EFS WEB ELECTRONIC FILING

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

TRANSMITTAL OF APPELLANT'S BRIEF ON APPEAL

Dear Sir:

Appellant submits herewith, Appellant's Brief on Appeal under 37 C.F.R. § 1.192 in support of the Notice of Appeal filed on February 24, 2009 in the above-identified application.

An appeal brief fee in the amount of $540.00 for filing this brief is submitted herewith via the Appellant's Attorneys' credit card. Appellant petitions the Commissioner for Patents to extend the time for filing this brief by one month so that the period for filing this brief is extended to May 24, 2009. An extension fee in the amount of $130.00 to cover the extension fee is submitted herewith via the Appellant's Attorneys' credit card.

The Commissioner is hereby authorized to credit overpayments or to charge any deficiency in a required fee to Deposit Account No. 19-3140.

Respectfully submitted,

Dated: May 26, 2009

By: /Adam C. Rehm/

Adam C. Rehm Reg. No. 54,797
SONNENSCHEIN NATH & ROSENTHAL
P.O. Box 061080
Wacker Drive Station, Sears Tower
Chicago, Illinois 60606-1080
(816) 460-2542

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Patent Application of: Takeo Eguchi			
Application No:	10/790,986	Group Art Unit:	2193
Filed:	March 2, 2004	Examiner	Chat C. Do
Customer No.:	26263		
For:	SIGNAL PROCESSING AND ERROR ACCUMULATION REDUCING APPARATUS, STORAGE MEDIUM STORING THEREON COMPUTER READABLE CODES TO CONTROL THE SIGNAL PROCESSING AND ERROR ACCUMULATION REDUCING APPARATUS, AND SIGNAL		

Via EFS WEB ELECTRONIC FILING

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

APPELLANT'S MAIN BRIEF ON APPEAL

Dear Sir:

In accordance with the provisions of 37 C.F.R. § 1.192, Appellant herewith submits this Main Brief in support of the Appeal for the above-referenced application.

I. REAL PARTY IN INTEREST

The real party in interest in the present appeal is the Assignee, Sony Corporation, a Japanese Corporation. The Assignment was recorded in the U.S. Patent and Trademark Office at Reel 015563, Frame 0892.

II. RELATED APPEALS AND INTERFERENCES

Appellant is not aware of any related appeals or interferences.

III. STATUS OF CLAIMS

Claims 1-4 and 9-20 were pending and under consideration. The remaining claims, i.e., claims 5-8, were previously cancelled. A copy of claims 1-4 and 9-20 is appended hereto as the Claims Appendix.

The present Appeal is directed to claims 1-4 and 9-20, which were finally rejected under 35 U.S.C. § 103(a) in an Office Action dated November 24, 2008.

The status of the claims on appeal is as follows:

A) Claims 1-4, 9-13, and 17-20 stand rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 4,272,648 to Agrawal, et al. in view of U.S. Patent Publication No. 2001/0025292 to Denk, et al.

B) Claims 14-16 stand rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 4,272,648 to Agrawal, et al. in view of U.S. Patent Publication No. 2001/0025292 to Denk, et al. and further in view of Admitted Prior Art.

IV. STATUS OF AMENDMENTS

All amendments have been entered in this application.

V. SUMMARY OF CLAIMED SUBJECT MATTER

In data signal processing, a result of processing performed on input data might produce a result that has a longer bit length than that of the input data. In this instance, it is necessary to adjust the result so as to have the same bit length as that of the input data. Such an adjustment

introduces an error into the final output, which causes degradation in frequency characteristics of the data signal.

In accordance with the present invention, continuously related, sequentially input data signals are processed with reduced bit length without degrading data signal frequency characteristics. The present general inventive concept accomplishes this by rounding off a bit length of each data signal to a desired length, calculating an error arising from the rounding off, and adding the error to a next data signal.

Claims 1, 9, and 13 are the only pending independent claims under consideration. Claims 2-4, 10-12, and 14-20 depend either directly or indirectly from one of independent claims 1 and 9.

Independent claims 1, 9, and 13 are summarized below. Independent claims 1, 9, and 13 are substantially similar except that claim 1 relates to an apparatus, claim 9 relates to a computer-readable medium, and claim 13 relates to a method. Nevertheless, the arguments presented in herein are equally relevant to each of independent claims 1, 9, and 13.

Claim 1 claims a signal processing apparatus 10 for receiving digital signals X that are continuously related and input sequentially, performing an operation (e.g., a calculation) on each of sequentially input digital signals X, and outputting a result Y of the operation (page 8, line 14 to page 9, line 3). The signal processing apparatus 10 includes: (1) operation means; (2) high-order part extraction means; (3) difference calculation means; and (4) feedback means.

(1) The operation means performs the predetermined operation on an input digital signal X, the operation means defined as a calculation means performing the following equation: $Y = 0.02X + 1$ (page 8, line 24 to page 9, line 3).

(2) The high-order part extraction means extracts a high-order part by rounding off a result of the operation performed by the operation means by rounding a value to a digit of an order which is higher than the lowest order digit of the value (page 9, line to page 11, line 1).

(3) The difference calculation means calculates the difference between the result of the operation performed by the operation means and the high-order part extracted by the high-order part extraction means (page 10, lines 3-12).

(4) The feedback means adds, to a next input digital signal X, the difference value calculated by the difference calculation means or a value obtained by performing a predetermined operation on the difference value calculated by the difference calculation means (page 11, lines 5-11).

Claim 9 claims a storage medium readable by a signal processing apparatus 10 and storing computer-readable codes to manage the signal processing apparatus 10 for receiving digital signals X that are continuously related and input sequentially, performing a predetermined operation on each of sequentially input digital signals, and outputting a result of the operation, the computer-readable codes causing the signal processing apparatus to function as: (1) operation means; (2) high-order part extraction means; (3) difference calculation means; and (4) feedback means (page 8, line 14 to page 9, line 3).

(1) The operation means performs the predetermined operation on an input digital signal X, the operation means defined as a calculation means performing the following equation: $Y = 0.02X + 1$ (page 8, line 24 to page 9, line 3).

(2) The high-order part extraction means extracts a high-order part by rounding off a result of the operation performed by the operation means by rounding a value to a digit of an order which is higher than the lowest order digit of the value (page 9, line to page 11, line 1).

(3) The difference calculation means calculates the difference between the result of the operation performed by the operation means and the high-order part extracted by the high-order part extraction means (page 10, lines 3-12).

(4) The feedback means adds, to a next input digital signal X, the difference value calculated by the difference calculation means or a value obtained by performing a

predetermined operation on the difference value calculated by the difference calculation means (page 11, lines 5-11).

Claim 13 claims a method for causing a signal processing apparatus 10 to be capable of receiving digital signals X that are continuously related and input sequentially, performing a predetermined operation on each of sequentially input digital signals X, and outputting a result of the operation, the method comprising (1) an operation step; (2) a high-order part extraction step; (3) a difference calculation step; and (4) a feedback step, which have been described above (page 8, line 14 to page 9, line 3).

(1) The operation step performs the predetermined operation on an input digital signal X, the operation step defined as performing the following equation: $Y = 0.02X + 1$ (page 8, line 24 to page 9, line 3).

(2) The high-order part extraction step extracts a high-order part by rounding off a result of the operation performed by the operation step by rounding a value to a digit of an order which is higher than the lowest order digit of the value (page 9, line to page 11, line 1).

(3) The difference calculation step calculates the difference between the result of the operation performed by the operation step and the high-order part extracted by the high-order part extraction step (page 10, lines 3-12).

(4) The feedback step adds, to a next input digital signal X, the difference value calculated by the difference calculation step or a value obtained by performing a predetermined operation on the difference value calculated by the difference calculation step (page 11, lines 5-11).

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

The following grounds of rejection are to be reviewed on appeal:

A) Whether Claims 1-4, 9-13, and 17-20 are patentable under 35 U.S.C. §103(a) a over U.S. Patent No. 4,272,648 to Agrawal, et al. and U.S. Patent Publication No. 2001/0025292 to Denk, et al.

B) Whether Claims 14-16 are patentable under 35 U.S.C. §103(a) over U.S. Patent No. 4,272,648 to Agrawal, et al., U.S. Patent Publication No. 2001/0025292 to Denk, et al. and Admitted Prior Art.

VII. ARGUMENT

A. Claims 1-4, 9-13, and 17-20 are patentable over U.S. Patent No. 4,272,648 to Agrawal, et al. and U.S. Patent Publication No. 2001/0025292 to Denk, et al.

Independent claims 1, 9, and 13 each recites, *inter alia*, "rounding off…wherein rounding off means rounding a value to a digit of an order which is higher than the lowest order digit of the value."

The Examiner acknowledges that Agrawal fails to disclose or suggest "rounding" and attempts to remedy this deficiency with Denk. However, Agrawal and Denk cannot be combined without destroying the intended purpose of Agrawal, and in any event, Denk teaches away from Agrawal.

Agrawal purports to provide increased accuracy with respect to gain control by truncating or chopping off a portion of a number and adding the truncated portion to another number. Specifically, Agrawal provides a process by which "[t]he output from the adder 62 is applied to a word length reduction circuit 63…[that] operates to provide the output signal Zn by simply discarding the M least significant bits." *See* Agrawal, Col. 7, Lns. 12-20. The least significant bits are then "employed via a feedback loop and are added to the next word product,

which is then used to provide a next output signal" thereby providing "extremely accurate gain control." *See* Agrawal, Abstract and Col. 7 Ln. 65-Col. 8 Ln 65.

Denk, on the other hand, discloses an "Apparatus and Method For Reducing Precision of Data." *See* Denk, Title. Because reducing precision is exactly the opposite of providing extreme accuracy, Denk teaches exactly the opposite of Agrawal. Additionally, Denk associates reducing precision with "rounding" by stating "rounding tends to introduce some form of precision reduction error." *See* Denk, para. 0041. Consequently, one of ordinary skill in the art would never have modified Agrawal with a process that would decrease accuracy such as "rounding," as argued by the Examiner, because such would destroy the intended purpose of Agrawal.

Further, the Examiner's logic for combining Agrawal and Denk is flawed. Particularly, the Examiner argues that one would "add the rounding off means…as seen in Denk…to minimize or eliminate error in reducing word length." *See* the Office Action, page 3. However, this logic is flawed for at least three reasons.

First, the passage relied on by the Examiner to support his logic is derived from Denk's "Summary of the Invention," which fails to provide any nexus between "rounding" and the remaining disclosure in Denk. Second, it is nonsensical to argue that one would use Denk's rounding to "minimize or eliminate error" because rounding does exactly the opposite by creating a less accurate result. As pointed out above, Denk teaches that rounding does exactly the opposite, i.e., "rounding tends to introduce some form of precision reduction error." *See* Denk, para. 0041. Third, if one considers the passage relied on in its entirety, one would view rounding as problematic and would never change Agrawal from a chopping-off process to a rounding process. Particularly, after providing a general overview of Denk, the alleged motivation reads, "[i]n this manner, errors due to rounding are minimized or eliminated." *See*

Denk, para. 0009. Clearly, the passage teaches away from rounding and one would not have modified Agrawal to round numbers in view of Denk.

For at least these reasons, the Examiner's logic for combining Agrawal and Denk is flawed.

In view of the foregoing, it is submitted that neither Agrawal nor Denk, individually or combined, disclose or fairly suggest all of the elements set forth in independent claims 1, 9, and 13, these claims are allowable over Agrawal and Denk. Likewise, claims 2-4, 10-12, and 14-20 depend from independent claim 1 or 9, include all of the elements of independent claim 1 or 9, and are allowable over Agrawal and Denk for at least the same reasons discussed above with respect to independent claim 1 or 9.

Accordingly, Appellant respectfully requests that the Board reverse the rejections of claims 1-4 and 9-20.

Respectfully submitted,

Dated: May 26, 2009

By: /Adam C. Rehm/

Adam C. Rehm Reg. No. 54,797
SONNENSCHEIN NATH & ROSENTHAL
P.O. Box 061080
Wacker Drive Station, Sears Tower
Chicago, Illinois 60606-1080
(816) 460-2542

VIII. CLAIMS APPENDIX

1. (Previously Presented) A signal processing apparatus for receiving digital signals that are continuously related and input sequentially, performing a predetermined operation on each of sequentially input digital signals, and outputting a result of the operation, the signal processing apparatus comprising:

operation means for performing the predetermined operation on an input digital signal;

high-order part extraction means for extracting a necessary high-order part by rounding off a result of the operation performed by the operation means;

difference calculation means for calculating the difference between the result of the operation performed by the operation means and the high-order part extracted by the high-order part extraction means; and

feedback means for adding, to a next input digital signal, the difference value calculated by the difference calculation means or a value obtained by performing a predetermined operation on the difference value calculated by the difference calculation means,

wherein rounding off means rounding a value to a digit of an order which is higher than the lowest order digit of the value.

2. (Original) A signal processing apparatus according to claim 1, wherein when a second set of continuously-related digital signals is sequentially input after completion of inputting of a first set of continuously-related digital signals, a difference value obtained as a result of the difference calculation performed, by the difference calculation means, on the last digital signal of the first set of digital signals or a value obtained by performing the predetermined operation on the difference value calculated by the difference means is reset to 0 or added with a particular value, and the resultant value is added, via the feedback means, to the first digital signal of the second digital signals.

3. (Original) A signal processing apparatus according to claim 1, wherein the feedback means adds, to the next input digital signal, a value obtained by multiplying the difference value calculated by the difference calculation means by a factor smaller than 1.

4. (Original) A signal processing apparatus according to claim 1, wherein a digital signal acquired by means of oversampling is input to the operation means.

5-8. (Cancelled)

9. (Previously Presented) A storage medium readable by a signal processing apparatus and storing computer-readable codes to manage the signal processing apparatus for receiving digital signals that are continuously related and input sequentially, performing a predetermined operation on each of sequentially input digital signals, and outputting a result of the operation, the computer-readable codes causing the signal processing apparatus to function as:

operation means for performing the predetermined operation on an input digital signal;

high-order part extraction means for extracting a necessary high-order part by rounding off a result of the operation performed by the operation means;

difference calculation means for calculating the difference between the result of the operation performed by the operation means and the high-order part extracted by the high-order part extraction means; and

feedback means for adding, to a next input digital signal, the difference value calculated by the difference calculation means or a value obtained by performing a predetermined operation on the difference value calculated by the difference calculation means,

wherein rounding off means rounding a value to a digit of an order which is higher than the lowest order digit of the value.

10. (Previously Presented) The storage medium storing computer-readable codes to manage the signal processing apparatus according to claim 9, wherein the program causes the signal processing apparatus to also function as means for controlling the value fed back to the input digital signal such that when a second set of continuously-related digital signals is sequentially input after completion of inputting of a first set of continuously-related digital signals, a difference value obtained as a result of the difference calculation performed, by the difference calculation means, on the last digital signal of the first set of digital signals or a value obtained by performing the predetermined operation on the difference value calculated by the difference means is reset to 0 or added with a particular value, and the resultant value is added, via the feedback means, to the first digital signal of the second digital signals.

11. (Previously Presented) The storage medium storing computer-readable codes to manage the signal processing apparatus according to claim 9, wherein the program causes the signal processing apparatus to also function as means for causing the feedback means to add, to the next input digital signal, a value obtained by multiplying the difference value calculated by the difference calculation means by a factor smaller than 1.

12. (Previously Presented) The storage medium storing computer-readable codes to manage the signal processing apparatus according to claim 9, wherein the program causes the signal processing apparatus to also function as means for inputting a digital signal acquired by means of oversampling to the operation means.

13. (Previously Presented) A method for causing a signal processing apparatus to be capable of receiving digital signals that are continuously related and input sequentially, performing a predetermined operation on each of sequentially input digital signals, and outputting a result of the operation, the method comprising:

an operation step of performing the predetermined operation on an input digital signal;

a high-order part extraction step of extracting a necessary high-order part by rounding off a result obtained in the operation step;

a difference calculation step of calculating the difference between the result obtained in the operation step and the high-order part extracted in the high-order part extraction step; and

a feedback step of adding, to a next input digital signal, the difference value calculated in the difference calculation step or a value obtained by performing a predetermined operation on the difference value calculated in the difference calculation step,

wherein rounding off means rounding a value to a digit of an order which is higher than the lowest order digit of the value.

14. (Previously Presented) The signal processing apparatus according to claim 1, further comprising:

low-order part extraction means for extracting a necessary low-order part by rounding off the result of the operation performed by the operation means,

wherein rounding off means rounding a value to a digit of an order which is higher than the lowest order digit of the value.

15. (Previously Presented) The signal processing apparatus according to claim 14, wherein if a lower-order value output from the lower-order part extraction means is equal to or greater than a predetermined factor, the lower-order value is rounded up to a high-order value

and added to an output of the high-order part extraction means.

16. (Previously Presented) The signal processing apparatus according to claim 1, wherein the rounding off a result of the operation performed by the operation means consists of rounding up if a rounded resultant is less than a predetermined figure.

17. (Previously Presented) The signal processing apparatus according to claim 1, wherein the rounding off a result of the operation performed by the operation means consists of rounding off if a rounded resultant is lower than a predetermined figure.

18. (Previously Presented) The signal processing apparatus according to claim 1, wherein an error is produced during the rounding off and the error is capable of being input to one of the high-order part extraction means and a low-order part extraction means depending on a factor.

19. (Previously Presented) The signal processing apparatus according to claim 18, wherein if an error is equal to or greater than a factor, then the error is input to the high-order part extraction means, and if the error is less than the factor, then the error is input to a low-order part extraction means.

20. (Previously Presented) The signal processing apparatus according to claim 1, wherein an error is produced if the result is not rounded up and is calculated via the difference calculation means and added to a next input digital signal via the feedback means.

IX. EVIDENCE APPENDIX

No evidence is submitted pursuant to §§ 1.130, 1.131, or 1.132 and no other evidence is relied upon.

X. RELATED PROCEEDINGS APPENDIX

Appellant is not aware of any related proceedings.